PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-164770
(43)Date of publication of application : 07.06.2002

(51)Int.Cl. H03K 5/12

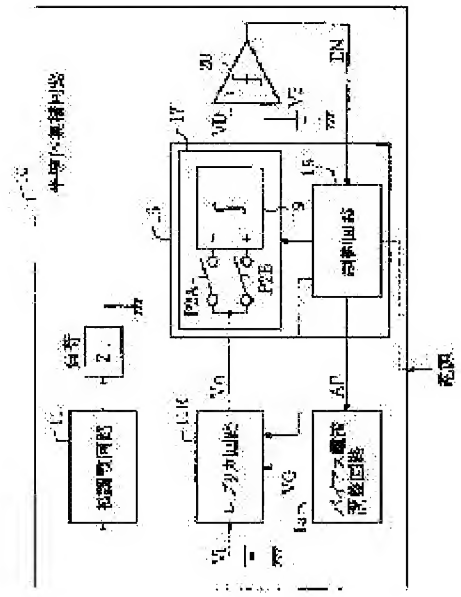
(21)Application number : 2000-357019
(22)Date of filing : 24.11.2000

(71)Applicant : FUJITSU LTD
(72)Inventor : NANBA HIROMI
MIZUTANI TORU
IKESHITA MAKOTO
TAKEYABU MASAHITO

(54) SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To save the power of a circuit more, in which the slew rate of an output depends on a bias current without adjusting the bias current before shipping a product.
SOLUTION: An evaluation circuit 16 repeats processing that its output is reset, that the difference of the output voltages Vo of a replica circuit 11R between after time t1 passes and after time t2 passes after performing step input of voltage Vi to the replica circuit 11R is calculated prescribed times and that these differences are accumulatively added. A comparator circuit 20 compares an accumulatively added voltages VD with a reference voltage VS. A bias adjustment circuit 15 steps up the bias current of the replica 11R and a circuit 11 to be adjusted in each of the prescribed number of times in the case of VD>VS and finishes adjustment in the case of VD<VS.

本発明の一実施形態の，出力のスルーレートがバイアス電流に依存する被調整回路及びバイアス電流自動調整回路を含む半導体集積回路のブロック図



CLAIMS

[Claim(s)]
[Claim 1]An integrated circuit comprising:
An equalization circuit for which a slew rate of an output depends on bias current.
A replica circuit of this equalization circuit through which bias current of the substantially same value as this bias current flows.
A weighting network which repeats processing in which accumulation of eye ********** and this difference is carried out for a difference with the 2nd output signal after the 2nd hour passes with the 1st output signal after the 1st hour passes after resetting an output and carrying out the step input of the predetermined value to this replica circuit.
A comparison circuit [preset value / value / this / that carried out accumulation], and a bias adjustment circuit to which this bias current is changed according to a comparison result of this comparison circuit for this every prescribed frequency.

[Claim 2]Have the following and this control circuit makes an integral value of (1) this subtraction and integration circuit reset, (2) Reset this replica circuit and, subsequently to this replica circuit, make a predetermined value input, This 1st hour of a rear stirrup which passed the 1st hour is made to supply to this subtraction and integration circuit after this input by making an output of this replica circuit into this 1st output signal until it passes, Subsequently, reset this replica circuit and, subsequently to this replica circuit, this predetermined value is made to input, The integrated circuit according to claim 1 characterized by what the above-mentioned prescribed frequency repetition, ** (1), and processing of (2) are repeated [a thing] for processing of making this 2nd hour of a rear stirrup which passed the 2nd hour supply to this subtraction and integration circuit after this input by making an output of this replica circuit into this 2nd output signal until it passes.
Subtraction and an integration circuit where the above-mentioned weighting network integrates with a difference of the 1st output signal of the above, and the 2nd output signal of the above
A control circuit.

[Claim 3]The above-mentioned bias adjustment circuit answers having been judged with the above-mentioned accumulation value being larger than the above-mentioned preset value by the above-mentioned comparison circuit, make it step up the above-mentioned bias current, and the above-mentioned control circuit, The integrated circuit according to claim 2 characterized by what it answers having been judged with this accumulation value being smaller than this preset value, and operation is suspended for.

[Claim 4]The above-mentioned bias adjustment circuit answers having been judged with the above-mentioned accumulation value being smaller than the above-mentioned preset value by the above-mentioned comparison circuit, carry out a step down, and the above-mentioned bias current the above-mentioned control circuit, The integrated circuit according to claim 2 characterized by what a judged thing with this larger accumulation value than this preset value is answered, and operation is suspended for.
[Claim 5]The above-mentioned bias adjustment circuit answers having been judged with the above-mentioned accumulation value being smaller than the above-mentioned preset value by the above-mentioned comparison circuit, and carries out the step down of the above-mentioned bias current, The integrated circuit according to claim 2 characterized by what answer a judged thing with this larger accumulation value than this preset value, and this bias current is made to step up, and operation is suspended for when the above-mentioned control circuit has an absolute value of a difference of this accumulation value and this preset value smaller than a predetermined value.
[Claim 6]The integrated circuit comprising according to claim 3:
The above-mentioned replica circuit is a complementary output type, and the above-mentioned subtraction and integration circuit are complementary input-and-output type arithmetic amplifiers.
The 1st capacitor connected between an inverted input end of this arithmetic amplifier, and a noninverting outgoing end.
The 2nd capacitor connected between a noninverting input end of this arithmetic amplifier, and an inverted output end.
A reset switch circuit which resets an electric charge of these 1st and 2nd capacitors, the 3rd and 4th capacitors and a complementary output of this replica circuit -- respectively -- this -- making the 3rd and this 4th capacitor charge, or making the 4th and 3rd capacitors charge, respectively -- subsequently -- this -- a switching circuit from which an electric charge of the 3rd and this 4th capacitor is moved to these 1st and 2nd capacitors, respectively.

[Claim 7]The integrated circuit comprising according to claim 6:
the above-mentioned subtraction and integration circuit connecting the 1st end of the 3rd and 4th capacitors of the above to reversal and a noninverting input end of the above-mentioned arithmetic amplifier, respectively, and making it into a tangent interlock state -- or -- respectively -- this arithmetic amplifier -- this -- noninverting and the 1st polarity changeover switch circuit which connect to an inverted input end and is changed into a reverse connection state.
The 2nd polarity changeover switch circuit which connects the 2nd end of the 3rd and 4th capacitors of the above to noninverting and an inverted output end of this arithmetic amplifier, respectively, and makes a tangent interlock state, or connects to this reversal and a noninverting outgoing end of this arithmetic amplifier, respectively, and is changed into a reverse connection state.

[Claim 8]The 1st period when both the above-mentioned control circuits make the above-mentioned 1st and 2nd polarity changeover switch circuit the above-mentioned tangent interlock state, The integrated circuit according to claim 7 repeating by turns the 2nd period that changes these both 1st and 2nd polarity changeover switch circuits into the above-mentioned reverse connection state, and performing the above-mentioned processing of the above (2) once in each of these 1st and 2nd periods.

[Claim 9]An integrated circuit of any one statement of claim 1 thru/or 7, wherein the above-mentioned equalization circuit has an arithmetic amplifier.
[Claim 10]The integrated circuit according to claim 9, wherein it is connected to an input stage of the above-mentioned arithmetic amplifier and the above-mentioned equalization circuit has a switched capacitor circuit further.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the integrated circuit in which the slew rate (variation of the output voltage per unit time) of an output includes the circuit which adjusts automatically the value of the equalization circuit depending on bias current, and this bias current.
[0002]
[Description of the Prior Art]Drawing 9 is a bias adjustment explanatory view of the conventional integrated circuit 10X in which the slew rate of an output includes the equalization circuit 11 depending on the bias current IB.
[0003]The bias current IB is supplied to the equalization circuit 11 from the bias circuit 12. The load impedance which the outgoing end of the equalization circuit 11 was connected to the output terminal of an unillustrated circuit or the integrated circuit 10X, and was seen from the outgoing end of the equalization circuit 11 is ZL.
[0004]Drawing 10 shows the sample hold circuit which combined the switched capacitor circuit and the operational amplifier 13X as the equalization circuit 11 in drawing 9. Drawing 10 shows the case where load impedance can approximate by capacity CL. Drawing 11 is a wave form chart showing operation of the circuit of drawing 10.
[0005]2 phase clock ** which shows drawing 11 the switch in drawing 10 -- 1 and ** -- it is controlled by 2 and a high level and low of a clock support the one and OFF of a switch which are controlled by the clock, respectively. the switch element P11, P12, and P13 -- clock ** -- being controlled by 1 -- the switch elements P21 and P22 -- clock ** -- it is controlled by 2.
[0006]The input-and-output voltage of the equalization circuit 11 is expressed with Vi and Vo, respectively. clock ** -- when 1 is a high level, the both ends of the capacitor C2 are grounded and reset, and the capacitor C1 is charged with the input voltage Vi. The charge quantity Q1 charged by the capacitor C1 is C1 and Vi. next, clock ** -- when 2 was set to a high level, this electric charge Q1 moves to the capacitor C2 and sufficient settling time is given, the charge quantity Q2 of the capacitor C2 serves as C2 and Vo. Since it is Q1=Q2, it is expressed Vo=(C1/C2) Vi.
[0007]If the equalization circuit 11 does not have sufficient driving ability to load-carrying-capacity CL when operating the equalization circuit 11 with a high-speed clock, a slew rate is insufficient, it is set to Vo<(C1/C2) Vi, and a required output swing is not obtained.
[0008]In a design, under the worst condition of the deviation of the circuit element characteristic generated in a manufacturing process, power supply voltage, and temperature, the bias current IB supplied to the operational amplifier 13X is determined so that a required output slew rate may be obtained. Under the present circumstances, the change of the driving ability of the operational amplifier 13X and the change of load-carrying-capacity CL accompanying change of the bias current IB are taken into consideration.

[0009]However, it does not usually become the worst conditions but becomes excess of power consumption.
[0010]Drawing 12 shows the output voltage Vo under the conditions from which the equalization circuit 11 manufactured based on the same design differs about the time t1-t3 in drawing 11. VLL shows the lower limit of the output voltage Vo required in order that the equalization circuit 11 may carry out normal operation under the worst conditions among drawing 12.
[0011]In order to return to drawing 9 and to solve the problem of this excess of power consumption in the former, The integrated circuit 10X is equipped with the bias circuit 12 which can adjust the bias current IB, The bias current IB of the same value as the bias current IB supplied to the equalization circuit 11 was taken out from the bias circuit 12 outside, and it measured with the ammeter 14, and trimming adjustment of adjusting the bias current IB with the equalization circuit 15X was performed so that this value might come in a prescribed range. This adjustment is performed in the culmination of manufacture of the integrated circuit 10X.
[0012]
[Problem(s) to be Solved by the Invention]However, since change of the value of the load impedance by change of the characteristic deviation or power supply voltage of load impedance, and temperature is not taken into consideration, the bias current IB must be determined supposing the maximum of load impedance, and it becomes insufficient saving the power. Since it is necessary to perform tuning of the bias current IB by the manufacturing stage of the integrated circuit 10X, it becomes a high cost.
[0013]The purpose of this invention is to provide the integrated circuit whose power can be saved more, without adjusting bias current for the circuit for which the slew rate of an output depends on bias current before product shipment in view of such a problem.
[0014]
[The means for solving a technical problem and its operation effect] In one mode of the integrated circuit by this invention, the slew rate of an output is provided with the replica circuit and bias current automatic regulation circuit of the equalization circuit depending on bias current, and repeat execution of the predetermined operation is carried out to this replica circuit for adjustment. This automatic regulation circuit has a weighting network, a comparison circuit, and a bias adjustment circuit.
[0015]In this weighting network, the output is reset and processing in which accumulation of eye ********** and this difference is carried out for a difference with the 2nd output signal after the 2nd hour passes with the 1st output signal after the 1st hour passes after carrying out the step input of the predetermined value to this replica circuit is repeated. This value that carried out accumulation is compared with a preset value in this comparison circuit. In this bias adjustment circuit, the bias current of this replica and this equalization circuit is similarly changed according to the comparison result of this comparison circuit for every bias adjustment circuit this prescribed frequency.
[0016]Since according to this integrated circuit bias current is suitably adjusted automatically according to it even if the bias current and output load of this equalization circuit have dispersion with a manufacturing deviation, power supply voltage, and ambient air temperature, power-saving is realizable. The parasitic capacitance of the circuit element of this automatic regulation circuit does not affect a main signal system including this equalization circuit, but moreover, it can adjust the bias current of this equalization circuit automatically in parallel with this, without stopping operation of this main signal system. It becomes unnecessary to perform bias current

tuning in the culmination of manufacture of this integrated circuit, and the cost can be reduced.
[0017]Other purposes, composition, and effects of this invention become clear from the following explanation.
[0018]
[Embodiment of the Invention]Hereafter, the embodiment of this invention is described with reference to drawings.
[0019][A 1st embodiment] Drawing 1 is a block diagram of the integrated circuit 10 in which the slew rate of an output includes the equalization circuit 11 and bias current automatic regulation circuit depending on bias current.
[0020]The load impedance which the outgoing end of the equalization circuit 11 was connected to the output terminal of other unillustrated circuits or the integrated circuit 10, and was seen from the outgoing end of the equalization circuit 11 is ZL. In the integrated circuit 10, the same replica circuit 11R is formed as substantially as the equalization circuit 11. In order to improve identity with the equalization circuit 11 more, the replica circuit 11R is formed near the equalization circuit 11. The bias current of the same value can flow into the equalization circuit 11 and the replica circuit 11R, and this value can be adjusted with the bias current equalization circuit 15. The weighting network 16 connected to the outgoing end of the replica circuit 11R is designed so that the load impedance seen from the outgoing end of the replica circuit 11R may become a value almost equal to it of the equalization circuit 11.
[0021]The weighting network 16 was provided with subtraction and the integration circuit 17, and the control circuit 18, and subtraction and the integration circuit 17 are provided with the switch element P2A, and 2B and the integration circuit 19.
[0022]The switch element P2A is connected between the outgoing end of the replica circuit 11R, and the inverted input end of the integration circuit 19, and switch element P2B is connected between the outgoing end of the replica circuit 11R, and the noninverting input end of the integration circuit 19. The integration circuit 19 is provided with an inverted input end and a noninverting input end, carries out accumulation of the value proportional to the difference of the signal supplied to the noninverting input end, and the signal supplied to the inverted input end, and outputs this as the difference accumulation voltage VD. Accumulation is carried out in order to raise bias current adjustment accuracy. That is, since this difference is very minute and it is difficult to carry out comparative evaluation of this directly in a tolerance, accumulation of this difference is carried out.
[0023]The difference accumulation voltage VD is supplied to the inverted input end of the comparator 20, and reference voltage VS is supplied to the noninverting input end of the comparator 20. The enable signal EN outputted from the comparator 20 is a low at the time of a high level and VD<VS at the time of VD>VS.
[0024]The control circuit 18 supplies a timing signal to the replica circuit 11R, and subtraction and an integration circuit 17, The replica circuit 11R, and subtraction and an integration circuit 17 are periodically operated like the after-mentioned, and if the enable signal EN is a high level after subtraction and the integration circuit 17 operate repeatedly N times (i.e., if it is VD>VS), the pulse of adjust signal AP will be supplied to the bias current equalization circuit 15. The bias current equalization circuit 15 answers this pulse, and adjusts one step of bias current of the replica circuit 11R and the equalization circuit 11 in the direction which that value converges on an optimum value.
[0025]Drawing 2 shows some examples of composition of drawing 1.
[0026]In the equalization circuit 11, the series connection of the circuit 21 and FET22 is carried

out between the power supply potential VDD and a ground. FET21R of the replica circuit 11R and 22R support FET21 of the equalization circuit 11, and 22, respectively.
[0027]The bias current equalization circuit 15 is provided with the counter 23 and D/A converter 24 with which the enumerated data are supplied, and the output of D/A converter 24 is supplied to the gate of FET22 and FET22R as gate voltage VG. The bias current IB according to the value of gate voltage VG flows into FET22 and FET22R. If gate voltage VG goes up, the bias current IB will increase and the output slew rate of the circuits 21 and 21R will become high.
[0028]In the control circuit 18, the clock CLK is supplied to the timing generating circuit 26 via the gate circuit 25. The timing generating circuit 26 generates the timing signal over the replica circuit 11R, and subtraction and an integration circuit 17 of drawing 1 based on this clock CLK. A pulse cycle generates judgment cycle signal JCS equal to a comparison test cycle (cycle judged at Step S7 of drawing 3 to be K=N), and supplies the timing generating circuit 26 to one input edge of AND gate 28 again. The enable signal EN is supplied to the input edge of another side of AND gate 28, and PASURU of judgment cycle signal JCS is supplied for the enable signal EN to clocked into end CK of the counter 23 as adjust signal AP via AND gate 28 between high level. If the gate circuit 25 will be in a through state to the clock CLK after powering on, this state is held at a flip-flop and the enable signal EN is set to a low in the pulse standup of judgment cycle signal JCS, This flip-flop will be reset, it will be in a cut off state to the clock CLK, and a stop, i.e., bias current automatic regulation operation, is completed by operation of the control circuit 18.
[0029]Drawing 3 is a flow chart which shows the sequence of control by the control circuit 18 of drawing 1. Drawing 4 (A) - (C) shows the ON-and-OFF waveform of the waveform of the output voltage Vo in drawing 1, the switch element P2A, and P2B. The inside of a parenthesis is [the following and] a step identification signal in drawing 3.
[0030](S1) The integration circuit 19 is reset and the output VD is set to 0V. The initial value 1 is loaded to inner counter K, and an initial value is loaded to the counter 23 of drawing 2.
[0031](S2) The replica circuit 11R is reset and the output voltage Vo is set to 0V.
[0032](S3) The step input of the input voltage Vi is carried out to the replica circuit 11R. This rises, as the output voltage Vo shows drawing 4 (A).
[0033](S4) If the number of the counters K is odd, it will progress to Step S5, and if the number is even, it will progress to Step S6.
[0034](S5) As shown in drawing 4 (A), switch element P2B is made one, and value Vo1 of the output voltage Vo in case switch element P2B changes from one at OFF is made to add to VD to the integration circuit 19 after carrying out the step input of the input voltage Vi to the replica circuit 11R until time t1 passes. Next, it progresses to Step S7.
[0035](S6) As shown in drawing 4 (A), the switch element P2A is made one, and value Vo2 of the output voltage Vo in case the switch element P2A changes from one at OFF is made to subtract from VD to the integration circuit 19 after carrying out the step input of the input voltage Vi to the replica circuit 11R until time t2 pass.
[0036](S7) If it is N<K, it will progress to Step S8, and if it is N=K, it will progress to step S9.
[0037](S8) Only 1 **********s the value of the counter K and it returns to Step S2.
[0038]Whenever it repeats processing of Steps S1-S8 twice, deltaV=Vo1-Vo2 is added to VD. Generally, the value proportional to difference voltage deltaV is added to VD.
[0039](S9) Judgment cycle signal JCS in drawing 2 rises, and if the enable signal EN is a high level ('H'), i.e., VD>VS, at this time, It progresses to Step S10, the clock CLK is not supplied to the timing generating circuit 26 in drawing 2, but operation of the control circuit 18 stops. Since

the pulse of adjust signal AP is no longer supplied to the counter 23 and the output of the counter 23 is fixed, gate voltage VG and the bias current IB are also fixed. Thereby, a bias current automatic regulation is completed.

[0040](S10) In drawing 2, the pulse of judgment cycle signal JCS passes along AND gate 28, and is supplied to clocked into end CK of the counter 23 as a pulse of adjust signal AP. Next, it returns to Step S1.

[0041]Drawing 4 (A) When the value of gate voltage VG corresponding to the waveform of the output voltage Vo of - (C) is expressed with VG1, VG2, and VG3, respectively, it is VG1<VG2<VG3. That is, the direction in the case of drawing 4 (B) has a value of the bias current IB larger than drawing 4 (A), and the direction in the case of drawing 4 (C) has a value of the bias current IB larger than drawing 4 (B). The build up time of the output voltage Vo becomes short, difference voltage deltaV becomes small, and the value of VD which integrated this N times also becomes small, so that the value of the bias current IB is large. Since power consumption becomes large so that the value of VD is small, the value of suitable VD which can prevent the excess of power consumption and in which the equalization circuit 11 carries out normal operation is calculated beforehand, and this value is set to reference voltage VS.

[0042]Gate voltage VG answers the pulse of adjust signal AP, and as shown in drawing 5 (A), it changes stair-like.

[0043]Since the integrated circuit 10 is equipped with the above bias current automatic regulation circuits to the equalization circuit 11 according to this embodiment, Even if the bias current and output load of the equalization circuit 11 have dispersion with a manufacturing deviation, power supply voltage, and ambient air temperature, according to it, bias current is adjusted automatically suitably, and power-saving can be realized. It becomes unnecessary to perform bias current tuning in the culmination of manufacture of the integrated circuit 10, and the cost can be reduced. Since it has the replica circuit 11R corresponding to the equalization circuit 11 and is adjusting automatically using the output, The bias current of the equalization circuit 11 can be adjusted automatically in parallel with this, without the parasitic capacitance of the circuit element of an automatic regulation circuit not affecting a main signal system, but moreover stopping operation of a main signal system.

[0044]Other methods may be adopted as completing the bias current IB. For example, the counter 23 is replaced with a down counter and it may be made to supply reference voltage VS and the difference accumulation voltage VD to the noninverting input end and inverted input end of the comparator 20 in drawing 1, respectively. In this case, gate voltage VG changes, as shown in drawing 5 (B). Whenever the pulse of judgment cycle signal JCS is supplied without using the counter 23 and AND gate 28 of drawing 2, Are 1 / method of 2 search, and it is made to change according to the numerals of the enable signal EN, as gate voltage VG is shown in drawing 5 (C), and it may be made to repeat this until the absolute value of the difference of the difference accumulation voltage VD and reference voltage VS turns into below the preset value epsilon.

[0045]Drawing 6 and drawing 7 show the example of composition of the replica circuit 11R in drawing 1, and subtraction and an integration circuit 17, respectively. These circuits are complementary input-and-output types. Drawing 8 shows the clock CLK, the control signal supplied to the circuit of drawing 6 and drawing 7, and judgment cycle signal JCS in drawing 2. Drawing 8 shows the case where the value of N in drawing 3 is 4.

[0046]This replica circuit 11R is a sample hold circuit which combined the switched capacitor circuit and the complementary input-and-output type operational amplifier 13, and is similar to the equalization circuit 11 of drawing 10. The same numerals as the corresponding thing in

drawing 10 are given to the switch element in drawing 6. In the circuit of drawing 6, it has P14 and P23 as a switch element which is not into drawing 10.
[0047]The switch element P14 is for short-circuiting between the inverted input end of the operational amplifier 13, and noninverting outgoing ends, and between a noninverting input end and inverted output ends at the time of reset of the replica circuit 11R, making complementary input and output of the operational amplifier 13 into same electric potential, for example, 1.4V, and setting offset to 0V. The switch element P23 is for separating the output of the operational amplifier 13 from the capacitors C21 and C22 at the time of this reset, and resetting the capacitors C21 and C22 to ground potential which is different in the operational amplifier 13.
[0048]clock [in drawing 8 to which the switch elements P11-P14 carried out 4 dividing of the clock CLK] ** -- ON-and-OFF control is carried out by 1 -- clock ** -- these switches are turned on when 1 is a high level. the switch elements P21-P23 -- clock ** -- clock [of 1 and an opposite phase] ** -- ON-and-OFF control is carried out by 2 -- clock ** -- these switches are turned on when 2 is a high level. The capacitors C11 and C12 are the same capacity value mutually, and are equivalent to the capacitor C1 of drawing 10. The capacitors C21 and C22 are the same capacity value mutually, and are equivalent to the capacitor C2 of drawing 10.
[0049]Vip=1.6V and Vim=1.2V are supplied to the replica circuit 11R as a complementary input signal.
[0050]Operation of the circuit of drawing 6 is drawing 10 mentioned above, and since he can understand easily, it omits the explanation.
[0051]Subtraction and the integration circuit 17 of drawing 7 are similar with the replica circuit 11R of drawing 6, The complementary input-and-output type operational amplifier 30, the polarity switching circuit 31, the switch element P15, the capacitors CL1 and CL2, C31 and C32, and the polarity switching circuit 32, respectively The operational amplifier 13 of drawing 6, the switch element P11, P21, the capacitor C11. And C12, C21 and C22, and the switch element P22 are supported.
[0052]The switch element P2A and P2B parallel and the polarity switching circuit 31 which carried out cross connection (right reverse connection), Where it was because addition and subtraction of charge quantity are enabled, and it made the switch element P23 one and the switch elements P15 and P16 are turned OFF, If the capacitors CL1 and CL2 are charged with the output voltage Vop and Vom, respectively, or the capacitors CL2 and CL1 are charged and then these electric charges are moved to the capacitors C31 and C32, addition and subtraction will be performed to the addition electric charge of the capacitors C31 and C32.
[0053]The capacity value of the capacitors CL1 and CL2 is set that the load impedance seen from the outgoing end of the circuit of drawing 6 becomes almost equal to the load impedance ZL in drawing 1.
[0054]The electric charge of the capacitors CL1 and CL2 moves to the capacitors C31 and C32, respectively, when the polarity switching circuits 32 and 33 turn OFF the switch element P23 by a positive or reverse connected state and make one the switch elements P15 and P16.
[0055]The polarity of the offset voltage which the polarity switching circuits 32 and 33 are the objects for offset voltage offset, and is added to the capacitors C31 and C32 when the polarity switching circuits 32 and 33 are made into a tangent interlock state and the electric charge of the capacitors CL1 and CL2 is moved to the capacitors C31 and C32, respectively, When the polarity switching circuits 32 and 33 are changed into a reverse connection state and the electric charge of the capacitors CL1 and CL2 is moved to the capacitors C31 and C32, respectively, the polarity of the offset voltage added to the capacitors C31 and C32 becomes reverse, and offset

voltage is offset.
[0056]The reset switch elements RSW1 and RSW2 are for resetting the electric charge of the capacitors C31 and C32.
[0057]the switch element P2A and P2B -- respectively -- clock [in drawing 8] ** -- it is controlled by 2A and clock ** 2B. the switch elements P15 and P16 -- the switch elements P11-P14 in drawing 6 -- clock [in drawing 8] ** -- it is controlled by 1. the switch element P23 -- the switch elements P21-P23 in drawing 6 -- clock [in drawing 8] ** -- it is controlled by 2. the switch elements P31 and P32 -- clock [in drawing 8] ** -- it is controlled by 3. the switch elements P41 and P42 -- clock [in drawing 8] ** -- it is controlled by 4. the reset switch elements RSW1 and RSW2 -- clock [in drawing 8] ** -- it is controlled by RST. Each clock for switch element control in drawing 8 supports the one and OFF of a switch element for which a high level and a low are controlled by this clock, respectively.
[0058]The difference voltage of the complementary output voltage VDp and VDm is equivalent to the difference accumulation voltage VD in drawing 1, and this is compared by reference voltage VS and the comparator 20 (drawing 1).
[0059]Next, operation of the circuit of drawing 7 is explained with reference to drawing 8.
[0060](t1-t2) The reset switch elements RSW1 and RSW2 are one, and the electric charge of the reset C31 and C32, i.e., capacitors, is reset for subtraction and the integration circuit 17.
[0061](t2-t9) The reset switch elements RSW1 and RSW2 are off. In time t2-t7, the switch elements P41 and P42 have one and the off switch elements P31 and P32, and it is this reverse in next time t7-t9.
[0062]The details of the time t2-t7 are as follows.
[0063](t3-t4) OFF and the switch elements P15 and P16 are [the switch element P2A / OFF and the switch element P23 of one and switch element P2B] one, and the capacitors CL1 and CL2 are charged with the output voltage Vop and Vom, respectively. The switch element P2A is come by off by t4, and the voltage of the output voltage Vop and Vom at this time is held at the capacitors CL1 and CL2, respectively.
[0064](t5-t6) The switch element P23 is OFF, the switch elements P15 and P16 are one, and the electric charge of the capacitors CL1 and CL2 moves to the capacitors C31 and C32, respectively.
[0065](t6-t7) One and the switch elements P15 and P16 are [the switch element P2A / OFF and the switch element P23 of OFF and switch element P2B] one, and the capacitors CL1 and CL2 are charged with the output voltage Vom and the output voltage Vop, respectively. Switch element P2B is come by off by t7, and the output voltage Vom at this time and the voltage of the output voltage Vop are held at the capacitors CL1 and CL2, respectively.
[0066]The details of the time t7-t10 are as follows.
[0067](t7-t8) The switch element P23 is OFF, the switch elements P15 and P16 are one, and the electric charge of the capacitors CL1 and CL2 moves to the capacitors C31 and C32, respectively.
[0068]In the time t8-t10, the same operation as the above t3-t8 is performed. However, just before the capacitors C31 and C32 are reset by t10, the pulse of judgment cycle signal JCS is outputted from the timing generating circuit 26 of drawing 2.
[0069]Operation explaining drawing 1 is performed by such operation.
[0070]Also outside, various modifications are included in this invention.
[0071]For example, not only a power up but when temperature or power supply voltage comes outside a setting range at the time of every fixed time and a system reset, it may be made to start

bias current automatic regulation processing. An output slew rate should just depend for the equalization circuit 11 on bias current.

TECHNICAL FIELD

[Field of the Invention]This invention relates to the integrated circuit in which the slew rate (variation of the output voltage per unit time) of an output includes the circuit which adjusts automatically the value of the equalization circuit depending on bias current, and this bias current.

PRIOR ART

[Description of the Prior Art]Drawing 9 is a bias adjustment explanatory view of the conventional integrated circuit 10X in which the slew rate of an output includes the equalization circuit 11 depending on the bias current IB.
[0003]The bias current IB is supplied to the equalization circuit 11 from the bias circuit 12. The load impedance which the outgoing end of the equalization circuit 11 was connected to the output terminal of an unillustrated circuit or the integrated circuit 10X, and was seen from the outgoing end of the equalization circuit 11 is ZL.
[0004]Drawing 10 shows the sample hold circuit which combined the switched capacitor circuit and the operational amplifier 13X as the equalization circuit 11 in drawing 9. Drawing 10 shows the case where load impedance can approximate by capacity CL. Drawing 11 is a wave form chart showing operation of the circuit of drawing 10.
[0005]2 phase clock ** which shows drawing 11 the switch in drawing 10 -- 1 and ** -- it is controlled by 2 and a high level and low of a clock support the one and OFF of a switch which are controlled by the clock, respectively. the switch element P11, P12, and P13 -- clock ** -- being controlled by 1 -- the switch elements P21 and P22 -- clock ** -- it is controlled by 2.
[0006]The input-and-output voltage of the equalization circuit 11 is expressed with Vi and Vo, respectively. clock ** -- when 1 is a high level, the both ends of the capacitor C2 are grounded and reset, and the capacitor C1 is charged with the input voltage Vi. The charge quantity Q1 charged by the capacitor C1 is C1 and Vi. next, clock ** -- when 2 was set to a high level, this electric charge Q1 moves to the capacitor C2 and sufficient settling time is given, the charge quantity Q2 of the capacitor C2 serves as C2 and Vo. Since it is Q1=Q2, it is expressed Vo=(C1/C2) Vi.
[0007]If the equalization circuit 11 does not have sufficient driving ability to load-carrying-capacity CL when operating the equalization circuit 11 with a high-speed clock, a slew rate is insufficient, it is set to Vo<(C1/C2) Vi, and a required output swing is not obtained.
[0008]In a design, under the worst condition of the deviation of the circuit element characteristic generated in a manufacturing process, power supply voltage, and temperature, the bias current IB supplied to the operational amplifier 13X is determined so that a required output slew rate may be obtained. Under the present circumstances, the change of the driving ability of the operational amplifier 13X and the change of load-carrying-capacity CL accompanying change of the bias current IB are taken into consideration.
[0009]However, it does not usually become the worst conditions but becomes excess of power consumption.
[0010]Drawing 12 shows the output voltage Vo under the conditions from which the

equalization circuit 11 manufactured based on the same design differs about the time t1-t3 in drawing 11. VLL shows the lower limit of the output voltage Vo required in order that the equalization circuit 11 may carry out normal operation under the worst conditions among drawing 12.

[0011]In order to return to drawing 9 and to solve the problem of this excess of power consumption in the former, The integrated circuit 10X is equipped with the bias circuit 12 which can adjust the bias current IB, The bias current IB of the same value as the bias current IB supplied to the equalization circuit 11 was taken out from the bias circuit 12 outside, and it measured with the ammeter 14, and trimming adjustment of adjusting the bias current IB with the equalization circuit 15X was performed so that this value might come in a prescribed range. This adjustment is performed in the culmination of manufacture of the integrated circuit 10X.

EFFECT OF THE INVENTION

[The means for solving a technical problem and its operation effect] In one mode of the integrated circuit by this invention, the slew rate of an output is provided with the replica circuit and bias current automatic regulation circuit of the equalization circuit depending on bias current, and repeat execution of the predetermined operation is carried out to this replica circuit for adjustment. This automatic regulation circuit has a weighting network, a comparison circuit, and a bias adjustment circuit.

[0015]In this weighting network, the output is reset and processing in which accumulation of eye ********** and this difference is carried out for a difference with the 2nd output signal after the 2nd hour passes with the 1st output signal after the 1st hour passes after carrying out the step input of the predetermined value to this replica circuit is repeated. This value that carried out accumulation is compared with a preset value in this comparison circuit. In this bias adjustment circuit, the bias current of this replica and this equalization circuit is similarly changed according to the comparison result of this comparison circuit for every bias adjustment circuit this prescribed frequency.

[0016]Since according to this integrated circuit bias current is suitably adjusted automatically according to it even if the bias current and output load of this equalization circuit have dispersion with a manufacturing deviation, power supply voltage, and ambient air temperature, power-saving is realizable. The parasitic capacitance of the circuit element of this automatic regulation circuit does not affect a main signal system including this equalization circuit, but moreover, it can adjust the bias current of this equalization circuit automatically in parallel with this, without stopping operation of this main signal system. It becomes unnecessary to perform bias current tuning in the culmination of manufacture of this integrated circuit, and the cost can be reduced.

[0017]Other purposes, composition, and effects of this invention become clear from the following explanation.

[0018]

[Embodiment of the Invention]Hereafter, the embodiment of this invention is described with reference to drawings.

[0019][A 1st embodiment] Drawing 1 is a block diagram of the integrated circuit 10 in which the slew rate of an output includes the equalization circuit 11 and bias current automatic regulation circuit depending on bias current.

[0020]The load impedance which the outgoing end of the equalization circuit 11 was connected to the output terminal of other unillustrated circuits or the integrated circuit 10, and was seen

from the outgoing end of the equalization circuit 11 is ZL. In the integrated circuit 10, the same replica circuit 11R is formed as substantially as the equalization circuit 11. In order to improve identity with the equalization circuit 11 more, the replica circuit 11R is formed near the equalization circuit 11. The bias current of the same value can flow into the equalization circuit 11 and the replica circuit 11R, and this value can be adjusted with the bias current equalization circuit 15. The weighting network 16 connected to the outgoing end of the replica circuit 11R is designed so that the load impedance seen from the outgoing end of the replica circuit 11R may become a value almost equal to it of the equalization circuit 11.

[0021]The weighting network 16 was provided with subtraction and the integration circuit 17, and the control circuit 18, and subtraction and the integration circuit 17 are provided with the switch element P2A, and 2B and the integration circuit 19.

[0022]The switch element P2A is connected between the outgoing end of the replica circuit 11R, and the inverted input end of the integration circuit 19, and switch element P2B is connected between the outgoing end of the replica circuit 11R, and the noninverting input end of the integration circuit 19. The integration circuit 19 is provided with an inverted input end and a noninverting input end, carries out accumulation of the value proportional to the difference of the signal supplied to the noninverting input end, and the signal supplied to the inverted input end, and outputs this as the difference accumulation voltage VD. Accumulation is carried out in order to raise bias current adjustment accuracy. That is, since this difference is very minute and it is difficult to carry out comparative evaluation of this directly in a tolerance, accumulation of this difference is carried out.

[0023]The difference accumulation voltage VD is supplied to the inverted input end of the comparator 20, and reference voltage VS is supplied to the noninverting input end of the comparator 20. The enable signal EN outputted from the comparator 20 is a low at the time of a high level and VD<VS at the time of VD>VS.

[0024]The control circuit 18 supplies a timing signal to the replica circuit 11R, and subtraction and an integration circuit 17, The replica circuit 11R, and subtraction and an integration circuit 17 are periodically operated like the after-mentioned, and if the enable signal EN is a high level after subtraction and the integration circuit 17 operate repeatedly N times (i.e., if it is VD>VS), the pulse of adjust signal AP will be supplied to the bias current equalization circuit 15. The bias current equalization circuit 15 answers this pulse, and adjusts one step of bias current of the replica circuit 11R and the equalization circuit 11 in the direction which that value converges on an optimum value.

[0025]Drawing 2 shows some examples of composition of drawing 1.

[0026]In the equalization circuit 11, the series connection of the circuit 21 and FET22 is carried out between the power supply potential VDD and a ground. FET21R of the replica circuit 11R and 22R support FET21 of the equalization circuit 11, and 22, respectively.

[0027]The bias current equalization circuit 15 is provided with the counter 23 and D/A converter 24 with which the enumerated data are supplied, and the output of D/A converter 24 is supplied to the gate of FET22 and FET22R as gate voltage VG. The bias current IB according to the value of gate voltage VG flows into FET22 and FET22R. If gate voltage VG goes up, the bias current IB will increase and the output slew rate of the circuits 21 and 21R will become high.

[0028]In the control circuit 18, the clock CLK is supplied to the timing generating circuit 26 via the gate circuit 25. The timing generating circuit 26 generates the timing signal over the replica circuit 11R, and subtraction and an integration circuit 17 of drawing 1 based on this clock CLK. A pulse cycle generates judgment cycle signal JCS equal to a comparison test cycle (cycle

judged at Step S7 of drawing 3 to be K=N), and supplies the timing generating circuit 26 to one input edge of AND gate 28 again. The enable signal EN is supplied to the input edge of another side of AND gate 28, and PASURU of judgment cycle signal JCS is supplied for the enable signal EN to clocked into end CK of the counter 23 as adjust signal AP via AND gate 28 between high level. If the gate circuit 25 will be in a through state to the clock CLK after powering on, this state is held at a flip-flop and the enable signal EN is set to a low in the pulse standup of judgment cycle signal JCS, This flip-flop will be reset, it will be in a cut off state to the clock CLK, and a stop, i.e., bias current automatic regulation operation, is completed by operation of the control circuit 18.

[0029]Drawing 3 is a flow chart which shows the sequence of control by the control circuit 18 of drawing 1. Drawing 4 (A) - (C) shows the ON-and-OFF waveform of the waveform of the output voltage Vo in drawing 1, the switch element P2A, and P2B. The inside of a parenthesis is [the following and] a step identification signal in drawing 3.

[0030](S1) The integration circuit 19 is reset and the output VD is set to 0V. The initial value 1 is loaded to inner counter K, and an initial value is loaded to the counter 23 of drawing 2.

[0031](S2) The replica circuit 11R is reset and the output voltage Vo is set to 0V.

[0032](S3) The step input of the input voltage Vi is carried out to the replica circuit 11R. This rises, as the output voltage Vo shows drawing 4 (A).

[0033](S4) If the number of the counters K is odd, it will progress to Step S5, and if the number is even, it will progress to Step S6.

[0034](S5) As shown in drawing 4 (A), switch element P2B is made one, and value Vo1 of the output voltage Vo in case switch element P2B changes from one at OFF is made to add to VD to the integration circuit 19 after carrying out the step input of the input voltage Vi to the replica circuit 11R until time t1 passes. Next, it progresses to Step S7.

[0035](S6) As shown in drawing 4 (A), the switch element P2A is made one, and value Vo2 of the output voltage Vo in case the switch element P2A changes from one at OFF is made to subtract from VD to the integration circuit 19 after carrying out the step input of the input voltage Vi to the replica circuit 11R until time t2 pass.

[0036](S7) If it is N<K, it will progress to Step S8, and if it is N=K, it will progress to step S9.

[0037](S8) Only 1 **********s the value of the counter K and it returns to Step S2.

[0038]Whenever it repeats processing of Steps S1-S8 twice, deltaV=Vo1-Vo2 is added to VD. Generally, the value proportional to difference voltage deltaV is added to VD.

[0039](S9) Judgment cycle signal JCS in drawing 2 rises, and if the enable signal EN is a high level ('H'), i.e., VD>VS, at this time, It progresses to Step S10, the clock CLK is not supplied to the timing generating circuit 26 in drawing 2, but operation of the control circuit 18 stops. Since the pulse of adjust signal AP is no longer supplied to the counter 23 and the output of the counter 23 is fixed, gate voltage VG and the bias current IB are also fixed. Thereby, a bias current automatic regulation is completed.

[0040](S10) In drawing 2, the pulse of judgment cycle signal JCS passes along AND gate 28, and is supplied to clocked into end CK of the counter 23 as a pulse of adjust signal AP. Next, it returns to Step S1.

[0041]Drawing 4 (A) When the value of gate voltage VG corresponding to the waveform of the output voltage Vo of - (C) is expressed with VG1, VG2, and VG3, respectively, it is VG1<VG2<VG3. That is, the direction in the case of drawing 4 (B) has a value of the bias current IB larger than drawing 4 (A), and the direction in the case of drawing 4 (C) has a value of the bias current IB larger than drawing 4 (B). The build up time of the output voltage Vo

becomes short, difference voltage deltaV becomes small, and the value of VD which integrated this N times also becomes small, so that the value of the bias current IB is large. Since power consumption becomes large so that the value of VD is small, the value of suitable VD which can prevent the excess of power consumption and in which the equalization circuit 11 carries out normal operation is calculated beforehand, and this value is set to reference voltage VS.
[0042]Gate voltage VG answers the pulse of adjust signal AP, and as shown in drawing 5 (A), it changes stair-like.
[0043]Since the integrated circuit 10 is equipped with the above bias current automatic regulation circuits to the equalization circuit 11 according to this embodiment, Even if the bias current and output load of the equalization circuit 11 have dispersion with a manufacturing deviation, power supply voltage, and ambient air temperature, according to it, bias current is adjusted automatically suitably, and power-saving can be realized. It becomes unnecessary to perform bias current tuning in the culmination of manufacture of the integrated circuit 10, and the cost can be reduced. Since it has the replica circuit 11R corresponding to the equalization circuit 11 and is adjusting automatically using the output, The bias current of the equalization circuit 11 can be adjusted automatically in parallel with this, without the parasitic capacitance of the circuit element of an automatic regulation circuit not affecting a main signal system, but moreover stopping operation of a main signal system.
[0044]Other methods may be adopted as completing the bias current IB. For example, the counter 23 is replaced with a down counter and it may be made to supply reference voltage VS and the difference accumulation voltage VD to the noninverting input end and inverted input end of the comparator 20 in drawing 1, respectively. In this case, gate voltage VG changes, as shown in drawing 5 (B). Whenever the pulse of judgment cycle signal JCS is supplied without using the counter 23 and AND gate 28 of drawing 2, Are 1 / method of 2 search, and it is made to change according to the numerals of the enable signal EN, as gate voltage VG is shown in drawing 5 (C), and it may be made to repeat this until the absolute value of the difference of the difference accumulation voltage VD and reference voltage VS turns into below the preset value epsilon.
[0045]Drawing 6 and drawing 7 show the example of composition of the replica circuit 11R in drawing 1, and subtraction and an integration circuit 17, respectively. These circuits are complementary input-and-output types. Drawing 8 shows the clock CLK, the control signal supplied to the circuit of drawing 6 and drawing 7, and judgment cycle signal JCS in drawing 2. Drawing 8 shows the case where the value of N in drawing 3 is 4.
[0046]This replica circuit 11R is a sample hold circuit which combined the switched capacitor circuit and the complementary input-and-output type operational amplifier 13, and is similar to the equalization circuit 11 of drawing 10. The same numerals as the corresponding thing in drawing 10 are given to the switch element in drawing 6. In the circuit of drawing 6, it has P14 and P23 as a switch element which is not into drawing 10.
[0047]The switch element P14 is for short-circuiting between the inverted input end of the operational amplifier 13, and noninverting outgoing ends, and between a noninverting input end and inverted output ends at the time of reset of the replica circuit 11R, making complementary input and output of the operational amplifier 13 into same electric potential, for example, 1.4V, and setting offset to 0V. The switch element P23 is for separating the output of the operational amplifier 13 from the capacitors C21 and C22 at the time of this reset, and resetting the capacitors C21 and C22 to ground potential which is different in the operational amplifier 13.
[0048]clock [in drawing 8 to which the switch elements P11-P14 carried out 4 dividing of the clock CLK] ** -- ON-and-OFF control is carried out by 1 -- clock ** -- these switches are

turned on when 1 is a high level. the switch elements P21-P23 -- clock ** -- clock [of 1 and an opposite phase] ** -- ON-and-OFF control is carried out by 2 -- clock ** -- these switches are turned on when 2 is a high level. The capacitors C11 and C12 are the same capacity value mutually, and are equivalent to the capacitor C1 of drawing 10. The capacitors C21 and C22 are the same capacity value mutually, and are equivalent to the capacitor C2 of drawing 10.
[0049]Vip=1.6V and Vim=1.2V are supplied to the replica circuit 11R as a complementary input signal.
[0050]Operation of the circuit of drawing 6 is drawing 10 mentioned above, and since he can understand easily, it omits the explanation.
[0051]Subtraction and the integration circuit 17 of drawing 7 are similar with the replica circuit 11R of drawing 6, The complementary input-and-output type operational amplifier 30, the polarity switching circuit 31, the switch element P15, the capacitors CL1 and CL2, C31 and C32, and the polarity switching circuit 32, respectively The operational amplifier 13 of drawing 6, the switch element P11, P21, the capacitor C11. And C12, C21 and C22, and the switch element P22 are supported.
[0052]The switch element P2A and P2B parallel and the polarity switching circuit 31 which carried out cross connection (right reverse connection), Where it was because addition and subtraction of charge quantity are enabled, and it made the switch element P23 one and the switch elements P15 and P16 are turned OFF, If the capacitors CL1 and CL2 are charged with the output voltage Vop and Vom, respectively, or the capacitors CL2 and CL1 are charged and then these electric charges are moved to the capacitors C31 and C32, addition and subtraction will be performed to the addition electric charge of the capacitors C31 and C32.
[0053]The capacity value of the capacitors CL1 and CL2 is set that the load impedance seen from the outgoing end of the circuit of drawing 6 becomes almost equal to the load impedance ZL in drawing 1.
[0054]The electric charge of the capacitors CL1 and CL2 moves to the capacitors C31 and C32, respectively, when the polarity switching circuits 32 and 33 turn OFF the switch element P23 by a positive or reverse connected state and make one the switch elements P15 and P16.
[0055]The polarity of the offset voltage which the polarity switching circuits 32 and 33 are the objects for offset voltage offset, and is added to the capacitors C31 and C32 when the polarity switching circuits 32 and 33 are made into a tangent interlock state and the electric charge of the capacitors CL1 and CL2 is moved to the capacitors C31 and C32, respectively, When the polarity switching circuits 32 and 33 are changed into a reverse connection state and the electric charge of the capacitors CL1 and CL2 is moved to the capacitors C31 and C32, respectively, the polarity of the offset voltage added to the capacitors C31 and C32 becomes reverse, and offset voltage is offset.
[0056]The reset switch elements RSW1 and RSW2 are for resetting the electric charge of the capacitors C31 and C32.
[0057]the switch element P2A and P2B -- respectively -- clock [in drawing 8] ** -- it is controlled by 2A and clock ** 2B. the switch elements P15 and P16 -- the switch elements P11-P14 in drawing 6 -- clock [in drawing 8] ** -- it is controlled by 1. the switch element P23 -- the switch elements P21-P23 in drawing 6 -- clock [in drawing 8] ** -- it is controlled by 2. the switch elements P31 and P32 -- clock [in drawing 8] ** -- it is controlled by 3. the switch elements P41 and P42 -- clock [in drawing 8] ** -- it is controlled by 4. the reset switch elements RSW1 and RSW2 -- clock [in drawing 8] ** -- it is controlled by RST. Each clock for switch element control in drawing 8 supports the one and OFF of a switch element for which a

high level and a low are controlled by this clock, respectively.
[0058]The difference voltage of the complementary output voltage VDp and VDm is equivalent to the difference accumulation voltage VD in drawing 1, and this is compared by reference voltage VS and the comparator 20 (drawing 1).
[0059]Next, operation of the circuit of drawing 7 is explained with reference to drawing 8.
[0060](t1-t2) The reset switch elements RSW1 and RSW2 are one, and the electric charge of the reset C31 and C32, i.e., capacitors, is reset for subtraction and the integration circuit 17.
[0061](t2-t9) The reset switch elements RSW1 and RSW2 are off. In time t2-t7, the switch elements P41 and P42 have one and the off switch elements P31 and P32, and it is this reverse in next time t7-t9.
[0062]The details of the time t2-t7 are as follows.
[0063](t3-t4) OFF and the switch elements P15 and P16 are [the switch element P2A / OFF and the switch element P23 of one and switch element P2B] one, and the capacitors CL1 and CL2 are charged with the output voltage Vop and Vom, respectively. The switch element P2A is come by off by t4, and the voltage of the output voltage Vop and Vom at this time is held at the capacitors CL1 and CL2, respectively.
[0064](t5-t6) The switch element P23 is OFF, the switch elements P15 and P16 are one, and the electric charge of the capacitors CL1 and CL2 moves to the capacitors C31 and C32, respectively.
[0065](t6-t7) One and the switch elements P15 and P16 are [the switch element P2A / OFF and the switch element P23 of OFF and switch element P2B] one, and the capacitors CL1 and CL2 are charged with the output voltage Vom and the output voltage Vop, respectively. Switch element P2B is come by off by t7, and the output voltage Vom at this time and the voltage of the output voltage Vop are held at the capacitors CL1 and CL2, respectively.
[0066]The details of the time t7-t10 are as follows.
[0067](t7-t8) The switch element P23 is OFF, the switch elements P15 and P16 are one, and the electric charge of the capacitors CL1 and CL2 moves to the capacitors C31 and C32, respectively.
[0068]In the time t8-t10, the same operation as the above t3-t8 is performed. However, just before the capacitors C31 and C32 are reset by t10, the pulse of judgment cycle signal JCS is outputted from the timing generating circuit 26 of drawing 2.
[0069]Operation explaining drawing 1 is performed by such operation.
[0070]Also outside, various modifications are included in this invention.
[0071]For example, not only a power up but when temperature or power supply voltage comes outside a setting range at the time of every fixed time and a system reset, it may be made to start bias current automatic regulation processing. An output slew rate should just depend for the equalization circuit 11 on bias current.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, since change of the value of the load impedance by change of the characteristic deviation or power supply voltage of load impedance, and temperature is not taken into consideration, the bias current IB must be determined supposing the maximum of load impedance, and it becomes insufficient saving the power. Since it is necessary to perform tuning of the bias current IB by the manufacturing stage of the integrated circuit 10X, it becomes a high cost.

[0013]The purpose of this invention is to provide the integrated circuit whose power can be saved more, without adjusting bias current for the circuit for which the slew rate of an output depends on bias current before product shipment in view of such a problem.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The slew rate of an output of one embodiment of this invention is a block diagram of an integrated circuit including the equalization circuit and bias current automatic regulation circuit depending on bias current.
[Drawing 2]It is a block diagram showing some examples of composition of drawing 1.
[Drawing 3]It is a flow chart which shows the sequence of control by the control circuit of drawing 1.
[Drawing 4](A) - (C) is all a figure showing the ON-and-OFF waveform of the waveform of the output voltage Vo in drawing 1, the switch element P2A, and P2B.
[Drawing 5](A) - (C) is a diagram showing the temporal response of the output value of the bias current equalization circuit in the case of adjusting bias current automatically with step-up, a step down, and 1/2 heuristics, respectively.
[Drawing 6]It is a figure showing the example of composition of the replica circuit in drawing 1.
[Drawing 7]It is a figure showing the example of composition of the subtraction and the integration circuit in drawing 1.
[Drawing 8]It is a timing chart which shows the reference clock CLK, the control signal supplied to the switch element of the circuit of drawing 6 and drawing 7, and judgment cycle signal JCS in drawing 2.
[Drawing 9]The slew rate of an output is a bias adjustment explanatory view of the conventional integrated circuit including the equalization circuit depending on bias current.
[Drawing 10]It is a figure showing the sample hold circuit which combined the switched capacitor circuit and operational amplifier as an equalization circuit in drawing 9.
[Drawing 11]It is a wave form chart showing operation of the circuit of drawing 10.
[Drawing 12]It is a figure showing the waveform of the output voltage Vo under the conditions from which the equalization circuit manufactured based on the same design differs about the time t1-t3 in drawing 11.
[Description of Notations]
10 Integrated circuit
11 Equalization circuit
11R Replica circuit
12 Bias circuit
13 and 30 Complementary input-and-output type operational amplifier
15 Bias current equalization circuit
16 Weighting network
17 Subtraction and an integration circuit
18 Control circuit
19 Integration circuit
20 Comparator
22, 22R FET
23 Counter

24 D/A converter
25 Gate circuit
26 Timing generating circuit
31-33 Polarity switching circuit

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号
特開2002－164770
（P2002－164770A）
(43)公開日　平成14年６月７日(2002.6.7)

(51)Int.Cl.[7]	識別記号	ＦＩ	ﾃｰﾏｺｰﾄﾞ（参考）
Ｈ０３Ｋ　5/12		Ｈ０３Ｋ　5/12	

審査請求　未請求　請求項の数10　ＯＬ　（全 10 頁）

(21)出願番号　特願2000－357019(P2000－357019)

(22)出願日　平成12年11月24日(2000.11.24)

(71)出願人　000005223
富士通株式会社
神奈川県川崎市中原区上小田中４丁目１番１号

(72)発明者　難波　広美
神奈川県川崎市中原区上小田中４丁目１番１号　富士通株式会社内

(72)発明者　水谷　徹
神奈川県川崎市中原区上小田中４丁目１番１号　富士通株式会社内

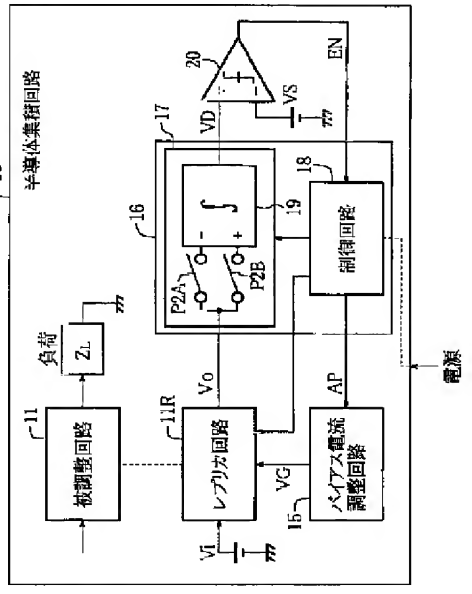
(74)代理人　100092587
弁理士　松本　眞吉

最終頁に続く

(54)【発明の名称】　半導体集積回路

(57)【要約】
【課題】出力のスルーレートがバイアス電流に依存する回路を、製品出荷前にバイアス電流の調整を行うことなく、より省電力化する。
【解決手段】評価回路１６では、その出力をリセットし、レプリカ回路１１Ｒに電圧Ｖｉをステップ入力してから時間ｔ１経過した後と時間ｔ２経過した後のレプリカ回路１１Ｒの出力電圧Ｖｏの差を所定回数求め、該差を累積加算する、という処理を繰り返す。比較回路２０では、累積加算電圧ＶＤを基準電圧ＶＳと比較する。バイアス調整回路１５は、該所定回数毎に、ＶＤ＞ＶＳであればレプリカ１１Ｒ及び被調整回路１１のバイアス電流をステップアップさせ、ＶＤ＜ＶＳであれば調整を終了する。

本発明の一実施形態の、出力のスルーレートがバイアス電流に依存する被調整回路及びバイアス電流自動調整回路を含む半導体集積回路のブロック図



【特許請求の範囲】
【請求項１】　出力のスルーレートがバイアス電流に依存する被調整回路と、
該バイアス電流と実質的に同じ値のバイアス電流が流れる、該被調整回路のレプリカ回路と、
出力をリセットし、該レプリカ回路に所定値をステップ入力してから第１時間経過した後の第１出力信号と第２時間経過した後の第２出力信号との差を所定回数求め、該差を累積加算する、という処理を繰り返す評価回路と、
この累積加算した値を設定値と比較する比較回路と、
該所定回数毎に、該比較回路の比較結果に応じて該バイアス電流を変化させるバイアス調整回路と、
を有することを特徴とする半導体集積回路。
【請求項２】　上記評価回路は、
上記第１出力信号と上記第２出力信号との差を積分する減算・積分回路と、
制御回路とを有し、該制御回路は、
（１）該減算・積分回路の積分値をリセットさせ、
（２）該レプリカ回路をリセットし、次いで該レプリカ回路に所定値を入力させ、この入力後、第１時間経過した後又は該第１時間経過するまで該レプリカ回路の出力を該第１出力信号として該減算・積分回路に供給させ、次いで該レプリカ回路をリセットし、次いで該レプリカ回路に該所定値を入力させ、この入力後、第２時間経過した後又は該第２時間経過するまで該レプリカ回路の出力を該第２出力信号として該減算・積分回路に供給させるという処理を上記所定回数繰り返し、
該（１）と（２）の処理を繰り返す、
ことを特徴とする請求項１記載の半導体集積回路。
【請求項３】　上記バイアス調整回路は、上記比較回路により上記累積加算値が上記設定値より大きいと判定されたことに応答して上記バイアス電流をステップアップさせ、
上記制御回路は、該累積加算値が該設定値より小さいと判定されたことに応答して動作を停止する、
ことを特徴とする請求項２記載の半導体集積回路。
【請求項４】　上記バイアス調整回路は、上記比較回路により上記累積加算値が上記設定値より小さいと判定されたことに応答して上記バイアス電流をステップダウンさせ、
上記制御回路は、該累積加算値が該設定値より大きい判定されたことに応答して動作を停止する、
ことを特徴とする請求項２記載の半導体集積回路。
【請求項５】　上記バイアス調整回路は、上記比較回路により上記累積加算値が上記設定値より小さいと判定されたことに応答して上記バイアス電流をステップダウンさせ、該累積加算値が該設定値より大きい判定されたことに応答して該バイアス電流をステップアップさせ、
上記制御回路は、該累積加算値と該設定値との差の絶対値が所定値より小さい場合に動作を停止する、
ことを特徴とする請求項２記載の半導体集積回路。
【請求項６】　上記レプリカ回路は相補出力型であり、
上記減算・積分回路は、
相補入出力型演算増幅回路と、
該演算増幅回路の反転入力端と非反転出力端との間に接続された第１キャパシタと、
該演算増幅回路の非反転入力端と反転出力端との間に接続された第２キャパシタと、
該第１及び第２キャパシタの電荷をリセットするリセットスイッチ回路と、
第３及び第４キャパシタと、
該レプリカ回路の相補出力でそれぞれ該第３及び該第４キャパシタを充電させ又はそれぞれ第４及び第３キャパシタを充電させ、次いで該第３及び該第４キャパシタの電荷をそれぞれ該第１及び第２キャパシタに移すスイッチ回路と、
を有することを特徴とする請求項３記載の半導体集積回路。
【請求項７】　上記減算・積分回路は、
上記第３及び第４キャパシタの第１端をそれぞれ上記演算増幅回路の反転及び非反転入力端に接続させて正接続状態にし又はそれぞれ該演算増幅回路の該非反転及び反転入力端に接続させて逆接続状態にする第１極性切換スイッチ回路と、
上記第３及び第４キャパシタの第２端をそれぞれ該演算増幅回路の非反転及び反転出力端に接続させて正接続状態にし又はそれぞれ該演算増幅回路の該反転及び非反転出力端に接続させて逆接続状態にする第２極性切換スイッチ回路と、
を有することを特徴とする請求項６記載の半導体集積回路。
【請求項８】　上記制御回路は、上記第１及び第２極性切換スイッチ回路を共に上記正接続状態にする第１期間と、該第１及び第２極性切換スイッチ回路を共に上記逆接続状態にする第２期間とを交互に繰り返し、該第１及び第２期間の各々において上記（２）の上記処理を１回行うことを特徴とする請求項７記載の半導体集積回路。
【請求項９】　上記被調整回路は、演算増幅回路を有することを特徴とする請求項１乃至７のいずれか１つに記載の半導体集積回路。
【請求項１０】　上記被調整回路はさらに、上記演算増幅回路の入力段に接続されスイッチトキャパシタ回路を有することを特徴とする請求項９記載の半導体集積回路。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、出力のスルーレート（単位時間当たりの出力電圧の変化量）がバイアス電流に依存する被調整回路及び該バイアス電流の値を自動

調整する回路を含む半導体集積回路に関する。
【０００２】
【従来の技術】図９は、出力のスルーレートがバイアス電流ＩＢに依存する被調整回路１１を含む従来の半導体集積回路１０Ｘのバイアス調整説明図である。
【０００３】被調整回路１１には、バイアス回路１２からバイアス電流ＩＢが供給される。被調整回路１１の出力端は不図示の回路又は半導体集積回路１０Ｘの出力端子に接続され、被調整回路１１の出力端から見た負荷インピーダンスはＺＬである。
【０００４】図１０は、図９中の被調整回路１１としての、スイッチトキャパシタ回路と演算増幅器１３Ｘとを組み合わせたサンプルホールド回路を示す。図１０では、負荷インピーダンスが容量ＣＬで近似できる場合を示している。図１１は、図１０の回路の動作を示す波形図である。
【０００５】図１０中のスイッチは、図１１に示す２相クロックΦ１及びΦ２で制御され、クロックの高レベル及び低レベルがそれぞれそのクロックで制御されるスイッチのオン及びオフに対応している。スイッチ素子Ｐ１１、Ｐ１２及びＰ１３はクロックΦ１で制御され、スイッチ素子Ｐ２１及びＰ２２はクロックΦ２で制御される。
【０００６】被調整回路１１の入出力電圧をそれぞれＶｉ及びＶｏで表す。クロックΦ１が高レベルのとき、キャパシタＣ２の両端が接地されてリセットされると共に、キャパシタＣ１が入力電圧Ｖｉで充電される。キャパシタＣ１に充電される電荷量Ｑ１は、Ｃ１・Ｖｉである。次にクロックΦ２が高レベルになると、この電荷Ｑ１がキャパシタＣ２へ移動し、充分なセットリング時間が与えられた場合には、キャパシタＣ２の電荷量Ｑ２はＣ２・Ｖｏとなる。Ｑ１＝Ｑ２であるので、Ｖｏ＝（Ｃ１／Ｃ２）Ｖｉと表される。
【０００７】被調整回路１１を高速クロックで動作させた場合、被調整回路１１が負荷容量ＣＬに対して充分な駆動能力を有しなければ、スルーレートが不足してＶｏ＜（Ｃ１／Ｃ２）Ｖｉとなり、必要な出力振幅が得られない。
【０００８】設計においては、製造過程で発生する回路素子特性の偏差、電源電圧及び温度の最悪条件下において、必要な出力スルーレートが得られるように、演算増幅器１３Ｘに供給するバイアス電流ＩＢが決定される。この際、バイアス電流ＩＢの変動に伴う演算増幅器１３Ｘの駆動能力の変動及び負荷容量ＣＬの変動が考慮される。
【０００９】しかし、通常は最悪条件にならず、消費電力過多となる。
【００１０】図１２は、同一設計に基づいて製造された被調整回路１１の異なる条件下での出力電圧Ｖｏを、図１１中の時間ｔ１～ｔ３について示す。図１２中、ＶＬは被調整回路１１が最悪条件下で正常動作するために必要な出力電圧Ｖｏの下限値を示す。
【００１１】図９に戻って、従来ではこの消費電力過多の問題を解決するために、バイアス電流ＩＢを調整可能なバイアス回路１２を半導体集積回路１０Ｘに備え、被調整回路１１に供給されるバイアス電流ＩＢと同じ値のバイアス電流ＩＢをバイアス回路１２から外部に取り出して電流計１４で測定し、この値が所定範囲内になるように、調整回路１５Ｘによりバイアス電流ＩＢを調整するというトリミング調整が行われていた。この調整は、半導体集積回路１０Ｘの製造の最終段階で行われる。
【００１２】
【発明が解決しようとする課題】しかし、負荷インピーダンスの特性偏差や電源電圧及び温度の変動による負荷インピーダンスの値の変化を考慮していないので、負荷インピーダンスの最大値を想定してバイアス電流ＩＢを決定しなければならず、省電力化が不十分となる。また、半導体集積回路１０Ｘの製造段階でバイアス電流ＩＢの調整作業を行う必要があるので、コスト高となる。
【００１３】本発明の目的は、このような問題点に鑑み、出力のスルーレートがバイアス電流に依存する回路を、製品出荷前にバイアス電流の調整を行うことなく、より省電力化することができる半導体集積回路を提供することにある。
【００１４】
【課題を解決するための手段及びその作用効果】本発明による半導体集積回路の一態様では、出力のスルーレートがバイアス電流に依存する被調整回路のレプリカ回路と、バイアス電流自動調整回路とを備え、調整のためにこのレプリカ回路に対し所定の動作を繰り返し実行させる。この自動調整回路は、評価回路と比較回路とバイアス調整回路とを有する。
【００１５】該評価回路では、その出力をリセットし、該レプリカ回路に所定値をステップ入力してから第１時間経過した後の第１出力信号と第２時間経過した後の第２出力信号との差を所定回数求め、該差を累積加算する、という処理を繰り返す。該比較回路では、この累積加算した値を設定値と比較する。該バイアス調整回路では、バイアス調整回路該所定回数毎に、該比較回路の比較結果に応じて該レプリカ及び該被調整回路のバイアス電流を同じように変化させる。
【００１６】この半導体集積回路によれば、製造偏差、電源電圧及び周囲温度により該被調整回路のバイアス電流及び出力負荷にばらつきがあっても、それに応じてバイアス電流が適当に自動調整されるので、省電力化が実現できる。また、該自動調整回路の回路素子の寄生容量は、該被調整回路を含む主信号系に影響を与えず、しかも、該主信号系の動作を止めることなくこれと平行して該被調整回路のバイアス電流を自動調整することができる。さらに、該半導体集積回路の製造の最終段階でバイ

アス電流調整作業を行う必要がなくなり、そのコストを低減することができる。

【００１７】本発明の他の目的、構成及び効果は以下の説明から明らかになる。

【００１８】

【発明の実施の形態】以下、図面を参照して本発明の実施形態を説明する。

【００１９】［第１実施形態］図１は、出力のスルーレートがバイアス電流に依存する被調整回路１１及びバイアス電流自動調整回路を含む半導体集積回路１０のブロック図である。

【００２０】被調整回路１１の出力端は、不図示の他の回路又は半導体集積回路１０の出力端子に接続され、被調整回路１１の出力端から見た負荷インピーダンスはＺＬである。半導体集積回路１０内には、被調整回路１１と実質的に同一のレプリカ回路１１Ｒが形成されている。被調整回路１１との同一性をより高めるために、レプリカ回路１１Ｒは被調整回路１１の近くに形成されている。被調整回路１１とレプリカ回路１１Ｒには同じ値のバイアス電流が流れ、この値はバイアス電流調整回路１５により調整可能となっている。レプリカ回路１１Ｒの出力端からみた負荷インピーダンスが被調整回路１１のそれにほぼ等しい値になるように、レプリカ回路１１Ｒの出力端に接続された評価回路１６が設計されている。

【００２１】評価回路１６は、減算・積分回路１７と制御回路１８とを備え、減算・積分回路１７はスイッチ素子Ｐ２Ａ及び２Ｂと積分回路１９とを備えている。

【００２２】スイッチ素子Ｐ２Ａは、レプリカ回路１１Ｒの出力端と積分回路１９の反転入力端との間に接続され、スイッチ素子Ｐ２Ｂは、レプリカ回路１１Ｒの出力端と積分回路１９の非反転入力端との間に接続されている。積分回路１９は、反転入力端と非反転入力端とを備え、非反転入力端に供給された信号と反転入力端に供給された信号との差に比例した値を累積加算し、これを差累積加算電圧ＶＤとして出力する。累積加算するのは、バイアス電流調整精度を高めるためである。すなわち、該差が極めて微小であり、許容誤差範囲内でこれを直接比較評価することが困難であるので、該差を累積加算する。

【００２３】差累積加算電圧ＶＤは比較器２０の反転入力端に供給され、比較器２０の非反転入力端には基準電圧ＶＳが供給される。比較器２０から出力されるイネーブル信号ＥＮは、ＶＤ＞ＶＳのとき高レベル、ＶＤ＜ＶＳのとき低レベルである。

【００２４】制御回路１８は、レプリカ回路１１Ｒ及び減算・積分回路１７に対しタイミング信号を供給して、レプリカ回路１１Ｒ及び減算・積分回路１７を後述のように周期的に動作させ、減算・積分回路１７がＮ回繰り返し動作した後にイネーブル信号ＥＮが高レベルであれば、すなわちＶＤ＞ＶＳであれば、バイアス電流調整回路１５に調整信号ＡＰのパルスを供給する。バイアス電流調整回路１５はこのパルスに応答して、レプリカ回路１１Ｒ及び被調整回路１１のバイアス電流を、その値が最適値に収束する方向へ１ステップ調整する。

【００２５】図２は、図１の一部の構成例を示す。

【００２６】被調整回路１１は、電源電位ＶＤＤとグランドとの間に回路２１とＦＥＴ２２とが直列接続されている。レプリカ回路１１ＲのＦＥＴ２１Ｒ及び２２Ｒはそれぞれ被調整回路１１のＦＥＴ２１及び２２に対応している。

【００２７】バイアス電流調整回路１５は、カウンタ２３と、その計数値が供給されるＤ／Ａ変換器２４とを備え、Ｄ／Ａ変換器２４の出力がゲート電圧ＶＧとしてＦＥＴ２２及びＦＥＴ２２Ｒのゲートに供給される。ＦＥＴ２２及びＦＥＴ２２Ｒには、ゲート電圧ＶＧの値に応じたバイアス電流ＩＢが流れる。ゲート電圧ＶＧが上昇すると、バイアス電流ＩＢが増加して回路２１及び２１Ｒの出力スルーレートが高くなる。

【００２８】制御回路１８では、クロックＣＬＫがゲート回路２５を介してタイミング発生回路２６に供給される。タイミング発生回路２６は、このクロックＣＬＫに基づいて、図１のレプリカ回路１１Ｒ及び減算・積分回路１７に対するタイミング信号を生成する。タイミング発生回路２６はまた、パルス周期が比較判定周期（図３のステップＳ７でＫ＝Ｎと判定される周期）に等しい判定サイクル信号ＪＣＳを生成してアンドゲート２８の一方の入力端に供給する。アンドゲート２８の他方の入力端にはイネーブル信号ＥＮが供給され、イネーブル信号ＥＮが高レベルの間、判定サイクル信号ＪＣＳのパスルがアンドゲート２８を介し調整信号ＡＰとしてカウンタ２３のクロック入力端ＣＫに供給される。ゲート回路２５は、電源投入後、クロックＣＬＫに対しスルー状態になり、この状態がフリップフロップに保持され、判定サイクル信号ＪＣＳのパルス立ち上がりでイネーブル信号ＥＮが低レベルになると、このフリップフロップがリセットされてクロックＣＬＫに対し遮断状態になり、制御回路１８の動作が停止、すなわちバイアス電流自動調整動作が完了する。

【００２９】図３は、図１の制御回路１８による制御のシーケンスを示すフローチャートである。図４（Ａ）～（Ｃ）は、図１中の出力電圧Ｖｏの波形並びにスイッチ素子Ｐ２Ａ及びＰ２Ｂのオン／オフ波形を示す。以下、括弧内は図３中のステップ識別符号である。

【００３０】（Ｓ１）積分回路１９をリセットしてその出力ＶＤを０Ｖにする。また、内部カウンタＫに初期値１をロードし、図２のカウンタ２３に初期値をロードする。

【００３１】（Ｓ２）レプリカ回路１１Ｒをリセットしてその出力電圧Ｖｏを０Ｖにする。

【００３２】（Ｓ３）レプリカ回路１１Ｒに対し、入力電圧Ｖｉをステップ入力させる。これにより、出力電圧Ｖｏが例えば図４（Ａ）に示す如く立ち上がる。
【００３３】（Ｓ４）カウンタＫが奇数であればステップＳ５へ進み、偶数であればステップＳ６へ進む。
【００３４】（Ｓ５）レプリカ回路１１Ｒに入力電圧Ｖｉをステップ入力してから時間ｔ１経過するまで、図４（Ａ）に示す如くスイッチ素子Ｐ２Ｂをオンにし、積分回路１９に対し、スイッチ素子Ｐ２Ｂがオンからオフに遷移する時の出力電圧Ｖｏの値Ｖｏ１をＶＤに加算させる。次にステップＳ７へ進む。
【００３５】（Ｓ６）レプリカ回路１１Ｒに入力電圧Ｖｉをステップ入力してから時間ｔ２経過するまで、図４（Ａ）に示す如くスイッチ素子Ｐ２Ａをオンにし、積分回路１９に対し、スイッチ素子Ｐ２Ａがオンからオフに遷移する時の出力電圧Ｖｏの値Ｖｏ２をＶＤから減算させる。
【００３６】（Ｓ７）Ｎ＜ＫであればステップＳ８へ進み、Ｎ＝ＫであればステップＳ９へ進む。
【００３７】（Ｓ８）カウンタＫの値を１だけインクリメントし、ステップＳ２へ戻る。
【００３８】ステップＳ１～Ｓ８の処理を２回繰り返す毎に、ΔＶ＝Ｖｏ１－Ｖｏ２がＶＤに加算される。一般には、差電圧ΔＶに比例した値がＶＤに加算される。
【００３９】（Ｓ９）図２中の判定サイクル信号ＪＣＳが立ち上がり、この時イネーブル信号ＥＮが高レベル（‘Ｈ’）、すなわちＶＤ＞ＶＳであれば、ステップＳ１０へ進み、そうでなければ図２においてクロックＣＬＫがタイミング発生回路２６に供給されず、制御回路１８の動作が停止する。調整信号ＡＰのパルスがカウンタ２３に供給されなくなり、カウンタ２３の出力が固定されるので、ゲート電圧ＶＧ及びバイアス電流ＩＢも固定される。これにより、バイアス電流自動調整が完了する。
【００４０】（Ｓ１０）図２において、判定サイクル信号ＪＣＳのパルスがアンドゲート２８を通り、調整信号ＡＰのパルスとしてカウンタ２３のクロック入力端ＣＫに供給される。次に、ステップＳ１へ戻る。
【００４１】図４（Ａ）～（Ｃ）の出力電圧Ｖｏの波形に対応するゲート電圧ＶＧの値をそれぞれＶＧ１、ＶＧ２及びＶＧ３で表すと、ＶＧ１＜ＶＧ２＜ＶＧ３である。すなわち、図４（Ａ）よりも図４（Ｂ）の場合の方がバイアス電流ＩＢの値が大きく、図４（Ｂ）よりも図４（Ｃ）の場合の方がバイアス電流ＩＢの値が大きい。バイアス電流ＩＢの値が大きいほど、出力電圧Ｖｏの立ち上がり時間が短くなって差電圧ΔＶが小さくなり、これをＮ回積算したＶＤの値も小さくなる。ＶＤの値が小さいほど消費電力が大きくなるので、消費電力過多を防止でき且つ被調整回路１１が正常動作する適当なＶＤの値を予め求めておき、この値を基準電圧ＶＳとしておく。
【００４２】ゲート電圧ＶＧは調整信号ＡＰのパルスに応答して、図５（Ａ）に示すように階段状に変化する。
【００４３】本実施形態によれば、被調整回路１１に対し上述のようなバイアス電流自動調整回路が半導体集積回路１０に備えられているので、製造偏差、電源電圧及び周囲温度により被調整回路１１のバイアス電流及び出力負荷にばらつきがあっても、それに応じてバイアス電流が適当に自動調整され、省電力化が実現できる。また、半導体集積回路１０の製造の最終段階でバイアス電流調整作業を行う必要がなくなり、そのコストを低減することができる。さらに、被調整回路１１に対応してレプリカ回路１１Ｒを備え、その出力を用いて自動調整を行っているので、自動調整回路の回路素子の寄生容量が主信号系に影響を与えず、しかも、主信号系の動作を止めることなくこれと平行して被調整回路１１のバイアス電流を自動調整することができる。
【００４４】なお、バイアス電流ＩＢを収束させるのに他の方法を採用してもよい。例えば、カウンタ２３をダウンカウンタで置き換え、図１中の比較器２０の非反転入力端及び反転入力端にそれぞれ基準電圧ＶＳ及び差累積加算電圧ＶＤを供給するようにしてもよい。この場合、ゲート電圧ＶＧは図５（Ｂ）に示すように変化する。また、図２のカウンタ２３及びアンドゲート２８を用いずに、判定サイクル信号ＪＣＳのパルスが供給される毎に、イネーブル信号ＥＮの符号に応じて１／２探索方でゲート電圧ＶＧを図５（Ｃ）に示す如く変化させ、差累積加算電圧ＶＤと基準電圧ＶＳとの差の絶対値が設定値ε以下になるまでこれを繰り返すようにしてもよい。
【００４５】図６及び図７はそれぞれ、図１中のレプリカ回路１１Ｒ及び減算・積分回路１７の構成例を示す。これらの回路は、相補入出力型である。図８は、クロックＣＬＫと、図６及び図７の回路に供給される制御信号と、図２中の判定サイクル信号ＪＣＳとを示す。図８は図３中のＮの値が４である場合を示している。
【００４６】このレプリカ回路１１Ｒは、スイッチトキャパシタ回路と相補入出力型演算増幅器１３とを組み合わせたサンプルホールド回路であり、図１０の被調整回路１１に類似している。図６中のスイッチ素子には、図１０中の対応するものと同じ符号を付している。図６の回路では、図１０中にないスイッチ素子として、Ｐ１４及びＰ２３を備えている。
【００４７】スイッチ素子Ｐ１４は、レプリカ回路１１Ｒのリセット時に演算増幅器１３の反転入力端と非反転出力端との間及び非反転入力端と反転出力端との間を短絡して、演算増幅器１３の相補入出力を同電位、例えば１．４Ｖにしてオフセットを０Ｖにするためのものである。スイッチ素子Ｐ２３は、このリセット時に演算増幅器１３の出力をキャパシタＣ２１及びＣ２２から切り離

して、キャパシタＣ２１及びＣ２２を演算増幅器１３とは異なるグランド電位にリセットするためである。

【００４８】スイッチ素子Ｐ１１～Ｐ１４は、クロックＣＬＫを４分周した図８中のクロックΦ１によりオン／オフ制御され、クロックΦ１が高レベルのときこれらスイッチがオンになる。スイッチ素子Ｐ２１～Ｐ２３は、クロックΦ１と逆相のクロックΦ２によりオン／オフ制御され、クロックΦ２が高レベルのときこれらスイッチがオンになる。キャパシタＣ１１及びＣ１２は互いに同一容量値であり、図１０のキャパシタＣ１に対応している。キャパシタＣ２１及びＣ２２は互いに同一容量値であり、図１０のキャパシタＣ２に対応している。

【００４９】レプリカ回路１１Ｒには、相補入力信号として例えばＶｉｐ＝１．６Ｖ、Ｖｉｍ＝１．２Ｖが供給される。

【００５０】図６の回路の動作は、上述した図１０のそれから容易に理解できるので、その説明を省略する。

【００５１】図７の減算・積分回路１７は、図６のレプリカ回路１１Ｒと類似しており、相補入出力型演算増幅器３０、極性切換回路３１、スイッチ素子Ｐ１５、キャパシタＣＬ１及びＣＬ２、Ｃ３１及びＣ３２、極性切換回路３２はそれぞれ図６の演算増幅器１３、スイッチ素子Ｐ１１、Ｐ２１、キャパシタＣ１１及びＣ１２、Ｃ２１及びＣ２２、スイッチ素子Ｐ２２に対応している。

【００５２】スイッチ素子Ｐ２Ａ及びＰ２Ｂを平行及びクロス接続（正逆接続）した極性切換回路３１は、電荷量の加減算を可能にするためのものであり、スイッチ素子Ｐ２３をオン、スイッチ素子Ｐ１５及びＰ１６をオフにした状態で、出力電圧Ｖｏｐ及びＶｏｍでそれぞれキャパシタＣＬ１及びＣＬ２を充電し又はキャパシタＣＬ２及びＣＬ１を充電して、次にこれらの電荷をキャパシタＣ３１及びＣ３２に移すと、キャパシタＣ３１及びＣ３２の積算電荷に対し加算及び減算が行われる。

【００５３】キャパシタＣＬ１及びＣＬ２の容量値は、図６の回路の出力端からみた負荷インピーダンスが図１中の負荷インピーダンスＺＬにほぼ等しくなるように定められる。

【００５４】キャパシタＣＬ１及びＣＬ２の電荷は、極性切換回路３２及び３３が正又は逆の接続状態でスイッチ素子Ｐ２３をオフにしスイッチ素子Ｐ１５及びＰ１６をオンにすることにより、それぞれキャパシタＣ３１及びＣ３２に移動する。

【００５５】極性切換回路３２及び３３はオフセット電圧相殺用であり、極性切換回路３２及び３３を正接続状態にしてキャパシタＣＬ１及びＣＬ２の電荷をそれぞれキャパシタＣ３１及びＣ３２に移した時にキャパシタＣ３１及びＣ３２に加算されるオフセット電圧の極性と、極性切換回路３２及び３３を逆接続状態にしてキャパシタＣＬ１及びＣＬ２の電荷をそれぞれキャパシタＣ３１及びＣ３２に移した時にキャパシタＣ３１及びＣ３２に加算されるオフセット電圧の極性とが逆になって、オフセット電圧が相殺される。

【００５６】リセットスイッチ素子ＲＳＷ１及びＲＳＷ２は、キャパシタＣ３１及びＣ３２の電荷をリセットするためのものである。

【００５７】スイッチ素子Ｐ２Ａ及びＰ２Ｂはそれぞれ図８中のクロックΦ２Ａ及びクロックΦ２Ｂにより制御される。スイッチ素子Ｐ１５及びＰ１６は、図６中のスイッチ素子Ｐ１１～Ｐ１４と共に図８中のクロックΦ１により制御される。スイッチ素子Ｐ２３は、図６中のスイッチ素子Ｐ２１～Ｐ２３と共に、図８中のクロックΦ２により制御される。スイッチ素子Ｐ３１及びＰ３２は図８中のクロックΦ３により制御される。スイッチ素子Ｐ４１及びＰ４２は図８中のクロックΦ４により制御される。リセットスイッチ素子ＲＳＷ１及びＲＳＷ２は図８中のクロックΦＲＳＴにより制御される。図８中のスイッチ素子制御用クロックはいずれも、高レベル及び低レベルがそれぞれこのクロックで制御されるスイッチ素子のオン及びオフに対応している。

【００５８】相補出力電圧ＶＤｐとＶＤｍの差電圧が図１中の差累積加算電圧ＶＤに対応しており、これが基準電圧ＶＳと比較器２０（図１）で比較される。

【００５９】次に、図７の回路の動作を、図８を参照して説明する。

【００６０】（ｔ１～ｔ２）リセットスイッチ素子ＲＳＷ１及びＲＳＷ２がオンであり、減算・積分回路１７がリセット、すなわちキャパシタＣ３１及びＣ３２の電荷がリセットされる。

【００６１】（ｔ２～ｔ９）リセットスイッチ素子ＲＳＷ１及びＲＳＷ２はオフである。時間ｔ２～ｔ７ではスイッチ素子Ｐ４１及びＰ４２がオン、スイッチ素子Ｐ３１及びＰ３２がオフであり、次の時間ｔ７～ｔ９ではこの逆である。

【００６２】時間ｔ２～ｔ７の詳細は次の通りである。

【００６３】（ｔ３～ｔ４）スイッチ素子Ｐ２Ａがオン、スイッチ素子Ｐ２Ｂがオフ、スイッチ素子Ｐ１５及びＰ１６がオフ、スイッチ素子Ｐ２３がオンであり、キャパシタＣＬ１及びＣＬ２がそれぞれ出力電圧Ｖｏｐ及びＶｏｍで充電される。ｔ４でスイッチ素子Ｐ２Ａがオフになり、この時の出力電圧Ｖｏｐ及びＶｏｍの電圧がそれぞれキャパシタＣＬ１及びＣＬ２に保持される。

【００６４】（ｔ５～ｔ６）スイッチ素子Ｐ２３がオフ、スイッチ素子Ｐ１５及びＰ１６がオンであり、キャパシタＣＬ１及びＣＬ２の電荷がそれぞれキャパシタＣ３１及びＣ３２に移動する。

【００６５】（ｔ６～ｔ７）スイッチ素子Ｐ２Ａがオフ、スイッチ素子Ｐ２Ｂがオン、スイッチ素子Ｐ１５及びＰ１６がオフ、スイッチ素子Ｐ２３がオンであり、キャパシタＣＬ１及びＣＬ２がそれぞれ出力電圧Ｖｏｍ及び出力電圧Ｖｏｐで充電される。ｔ７でスイッチ素子Ｐ

２Ｂがオフになり、この時の出力電圧Ｖｏｍ及び出力電圧Ｖｏｐの電圧がそれぞれキャパシタＣＬ１及びＣＬ２に保持される。

【００６６】時間ｔ７～ｔ１０の詳細は、次の通りである。

【００６７】（ｔ７～ｔ８）スイッチ素子Ｐ２３がオフ、スイッチ素子Ｐ１５及びＰ１６がオンであり、キャパシタＣＬ１及びＣＬ２の電荷がそれぞれキャパシタＣ３１及びＣ３２に移動する。

【００６８】時間ｔ８～ｔ１０においては、上記ｔ３～ｔ８と同様な動作が行われる。但し、ｔ１０でキャパシタＣ３１及びＣ３２がリセットされる直前に、判定サイクル信号ＪＣＳのパルスが図２のタイミング発生回路２６から出力される。

【００６９】このような動作により、図１について説明した動作が実行される。

【００７０】なお、本発明には外にも種々の変形例が含まれる。

【００７１】例えば、バイアス電流自動調整処理は、電源投入時のみならず、一定時間おき、システムリセット時、温度又は電源電圧が設定範囲外になった時などに開始するようにしてもよい。また、被調整回路１１は、出力スルーレートがバイアス電流に依存するものであればよい。

【図面の簡単な説明】

【図１】本発明の一実施形態の、出力のスルーレートがバイアス電流に依存する被調整回路及びバイアス電流自動調整回路を含む半導体集積回路のブロック図である。

【図２】図１の一部の構成例を示すブロック図である。

【図３】図１の制御回路による制御のシーケンスを示すフローチャートである。

【図４】（Ａ）～（Ｃ）はいずれも、図１中の出力電圧Ｖｏの波形並びにスイッチ素子Ｐ２Ａ及びＰ２Ｂのオン／オフ波形を示す図である。

【図５】（Ａ）～（Ｃ）はそれぞれステップアップ、ステップダウン及び１／２探索法でバイアス電流を自動調整する場合のバイアス電流調整回路の出力値の時間的変化を示す線図である。

【図６】図１中のレプリカ回路の構成例を示す図である。

【図７】図１中の減算・積分回路の構成例を示す図である。

【図８】基準クロックＣＬＫと、図６及び図７の回路のスイッチ素子に供給される制御信号と、図２中の判定サイクル信号ＪＣＳとを示すタイミングチャートである。

【図９】出力のスルーレートがバイアス電流に依存する被調整回路を含む従来の半導体集積回路のバイアス調整説明図である。

【図１０】図９中の被調整回路としての、スイッチトキャパシタ回路と演算増幅器とを組み合わせたサンプルホールド回路を示す図である。

【図１１】図１０の回路の動作を示す波形図である。

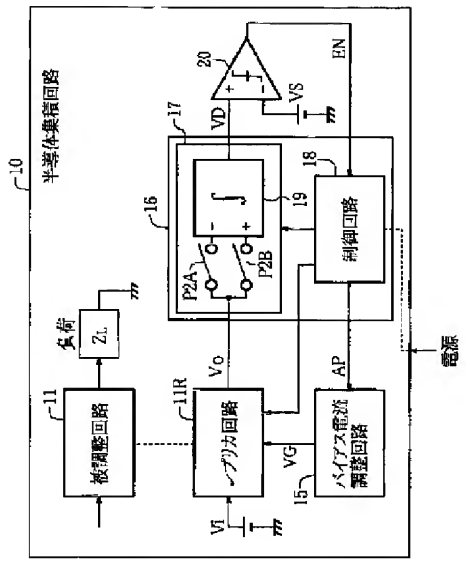
【図１２】同一設計に基づいて製造された被調整回路の異なる条件下での出力電圧Ｖｏの波形を、図１１中の時間ｔ１～ｔ３について示す図である。

【符号の説明】

１０　半導体集積回路
１１　被調整回路
１１Ｒ　レプリカ回路
１２　バイアス回路
１３、３０　相補入出力型演算増幅器
１５　バイアス電流調整回路
１６　評価回路
１７　減算・積分回路
１８　制御回路
１９　積分回路
２０　比較器
２２、２２Ｒ　ＦＥＴ
２３　カウンタ
２４　Ｄ／Ａ変換器
２５　ゲート回路
２６　タイミング発生回路
３１～３３　極性切換回路

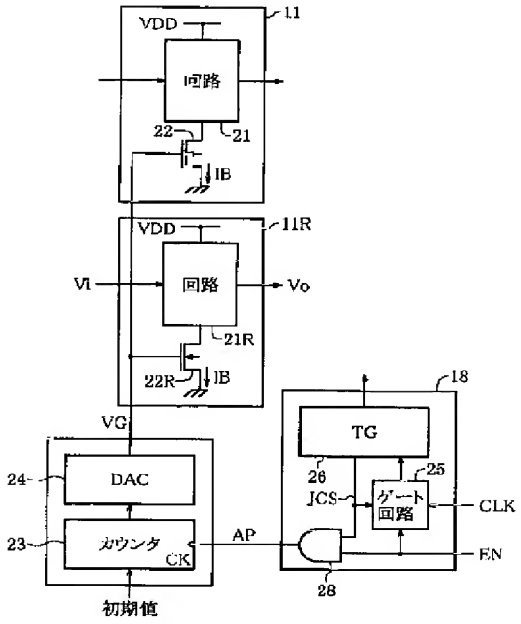
【図1】

本発明の一実施形態の、出力のスルーレートがバイアス電流に依存する被調整回路及びバイアス電流自動調整回路を含む半導体集積回路のブロック図



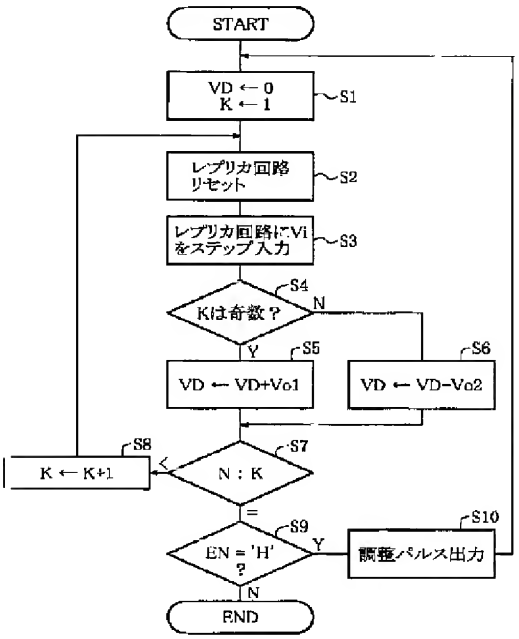
【図2】

図1の一部の構成例を示すブロック図



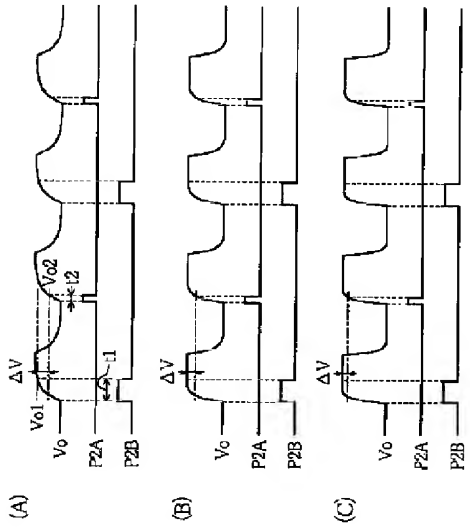
【図3】

図1の制御回路による制御のシーケンスを示すフローチャート



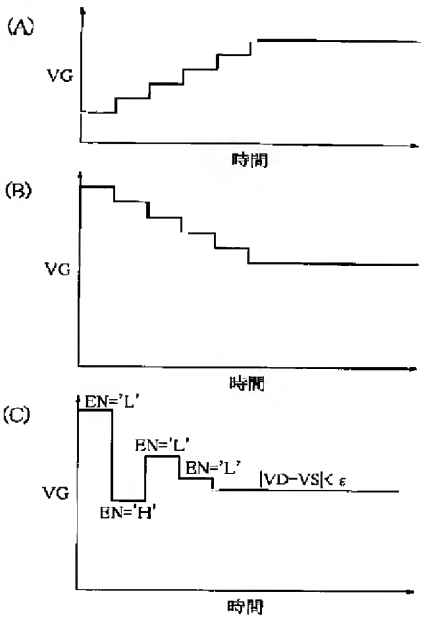
【図4】

(A)～(C)はいずれも、図1中の出力電圧Voの波形並びにスイッチ素子P2A及びP2Bのオン／オフ波形を示す図



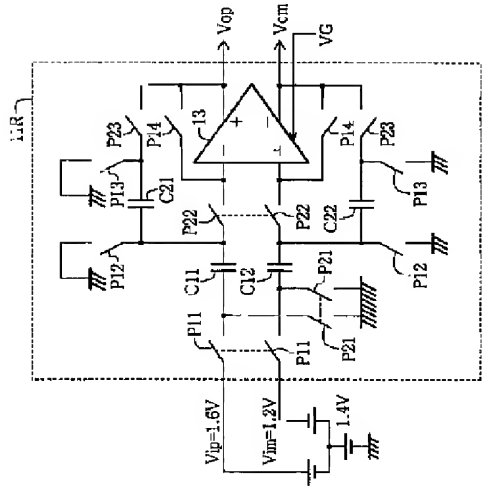
【図5】

(A)～(C)はそれぞれステップアップ、ステップダウン及び1／2探索法でバイアス電流を自動調整する場合のバイアス電流調整回路の出力値の時間的変化を示す線図



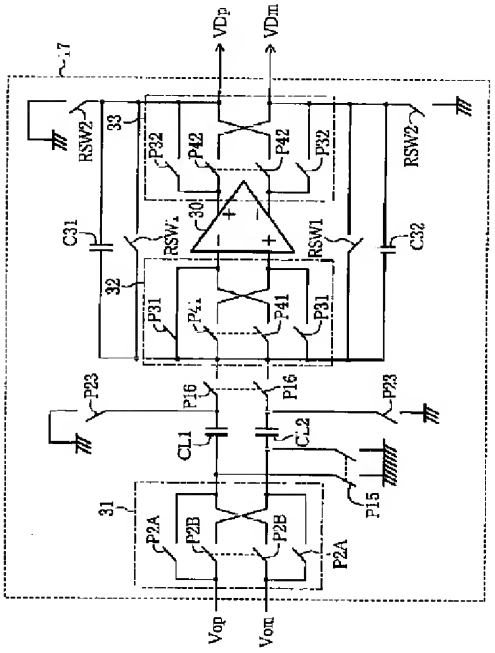
【図6】

図1中のレプリカ回路の構成例を示す図



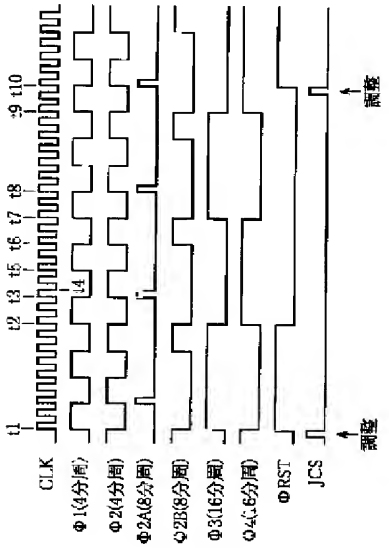
【図7】

図1中の減算・積分回路の構成例を示す図



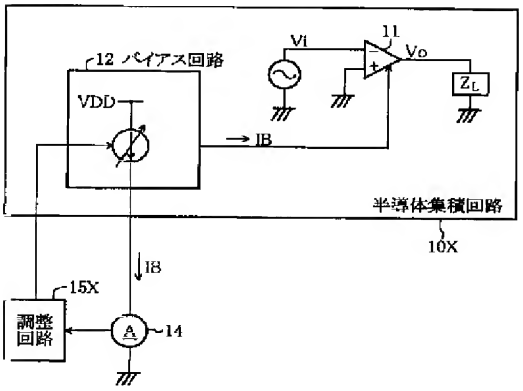
【図8】

基準クロックCLKと、図6及び図7の回路のスイッチ素子に供給される制御信号と、図2中の判定サイクル信号JCSとを示すタイミングチャート



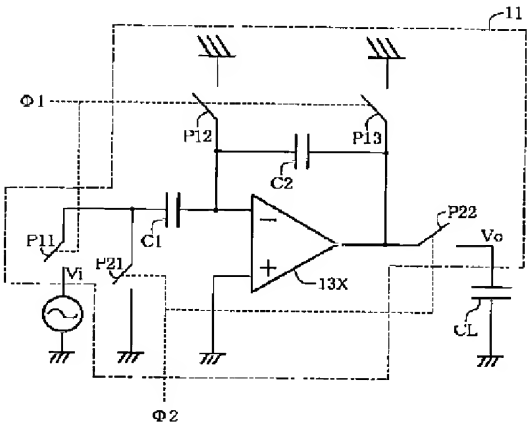
【図９】

出力のスルーレートがバイアス電流に依存する被調整回路を含む従来の半導体集積回路のバイアス調整説明図



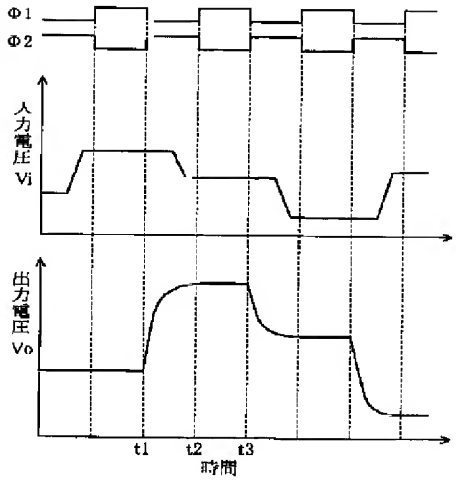
【図１０】

図9中の被調整回路としての、スイッチトキャパシタ回路と演算増幅器とを組み合わせたサンプルホールド回路を示す図



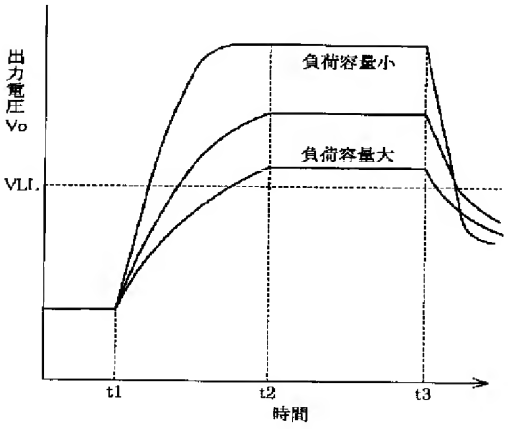
【図１１】

図10の回路の動作を示す波形図



【図１２】

同一設計に基づいて製造された被調整回路の異なる条件下での出力電圧Voの波形を、図11中の時間t1～t3について示す図



フロントページの続き

(72)発明者　池下　良
北海道札幌市北区北七条西四丁目３番地１号　富士通北海道ディジタル・テクノロジ株式会社内

(72)発明者　竹藪　雅人
北海道札幌市北区北七条西四丁目３番地１号　富士通北海道ディジタル・テクノロジ株式会社内